A process for fabricaling a thin-film device: forming a conducting layer composed of an said Process comprising the steps of: etching said conducting layer to form a etching said conducting said conducting layer to form a etching said conducting said conductin anodically oxidizable metal on a substrate; Plurality or pus lines naving upper surfaces and connection side surfaces and lines and inclined side surfaces and lines and substrate and inclined to eaid him and horizons electrically connected to eaid him portions electrically connected to eaid him and him an sala supstrate and inclined side surfaces and connectic to said bus lines and connected to said bus trate and connected to said substrate and portions electrically narallal to said substrate and portions electricate narallal to said substrate and portions electricates narallal to said substrate and inclined substrate and inclined substrate and connectic substrate and connectic substrate and connectic substrate substrate substrate and connectic substrate substrat Portions electrically connected to said substrate and portions electrically parallel to said substrate and portions upper surfaces. And inclined side surfaces. anodically oxidizing said bus lines and call another said bus lines and ca anodically oxidizing said bus lines and said oxidizing said bus lines and said connection portions include inner conduction nortions include inner conduction nortions include inner conduction nortions sala connection portions include inner convering portions and connection portions include films covering said inner convering portions include films covering said inner covering outer insulating oxide films covering covering outer insulating oxide films covering said inner covering sai 5 inclined side surfaces; and connection portions include inner conducting portions include inner covering said inner outer insulating oxide films covering said inner outer insulating portions of the films covering said inner outer insulating portions of the films covering said inner outer insulating portions of the films covering said inner outer insulating portions of the films covering said inner outer insulating portions of the films covering said inner outer insulating portions in the films covering said inner outer insulating portions in the films covering said inner outer insulating portions in the films covering said inner outer insulating outer insulating portions in the films covering said inner outer insulating o respectively claim 1, wherein said according to claim 1, wherein said A process according to claim 1, wherein said of the side surfaces of that the side connection of said connection is carried out so that and side surfaces of said connection etching lines and the side surfaces of said bus lines and the side surfaces of the side surfaces of said bus lines and the side said bus lines are said bus lines and the side said bus lines are said bus lines and the side said bus lines are said bus lines and the side said bus lines are said bus lines and the side said bus lines are said bus lines and the side said bus lines are said bus lines and the side said bus lines are said bus lines and the side said bus lines are said bus lines and the side said bus lines are said bus lines are said bu etcning step is carried out so that the said connection of said the said bus lines inclined at angles within the range from some said bus are inclined at angles within the said the said bus are inclined at angles within the said connection. sala pus lines and the side surfaces within the range from and the side surfaces within the range from the rang portions are inclined at angles within the range to said degrees; an average; with respect to said degrees. outer the portions conducting Portions A Process acobrding to claim 21 wherein said A process according to claim 2, wherein said of that the side surfaces of that the side connection of said out so that an feath connection etching lines and the side surfaces of said bus lines and the said bus lines are said bus lines and the said bus lines are said bus lines and the said bus lines are said bus lines and the said bus lines are said bus lines and the said bus lines are said bus lines and the said bus lines are said bus lines are said bus lines are said bus lines and the said bus lines are said bus lines ercning step is and the side surfaces of that the side connection out so that the said connection at annies within the range from it in the said bus lines inclined at annies portions are inclined at annies within the said bus are inclined at annies within the said connection. sald Dus lines and the side surfaces of sald connection 30 the range from 30 the ran 15 portions are inclined at angles within the range to said degrees, an average, with respect to said degrees. 4. A process according to claim 1, further conducting to claim 1, further ashing a mask on said conducting to claim 1, further conducting to claim 1, furth substrate. comprising the step for forming a mask on said conducting and the step for ashing and the said mask between said mask layer prior to layer substrate including said mask said mask said substrate 20 5. A process according to claim 1, further said conducting to claim 1, further to claim 1, further to claim 1, further to claim 1, further to said conducting to claim 1, further to said conducting to claim 1, further to said conducting to claim 1, further to conduct the said conducting to claim 1, further to conduct the said conducting to claim 1, further to conduct the said conducting to claim 1, further to conduct the said conducting to claim 1, further to conduct the said conducting to claim 1, further to claim 1, fur substrate. comprising the step for baking said mask prior haking said layer and the wherein the temperature for haking said the step for the temperature for haking said mask prior haking said ma saru mean reference and said etching step. layer and the step tor paking said mask prior to said the temperature for baking said wherein the temperature etching step! said substrate 30 35

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mask in said baking step is so set that said mask will have a relatively small rigidity so that an outer portion of said mask is pushed up from said conducting layer due to a reaction gas in said etching step.

6. A process according to claim 5, wherein the temperature for baking said mask in said baking step is not higher than 115°C.

- 7. A process according to claim 5, wherein said etching step is carried out so that the side surfaces of said bus lines and the side surfaces of said connection portions are outwardly convex.
- 8. A process according to claim 5, wherein said etching step is carried out so that the angles between the upper surfaces and the side surfaces of said bus lines and of said connection portions are obtuse angles.
- 9. A process according to claim 1, further comprising an ionic milling step for removing part of the outer oxide films to expose the inner conducting portions after said step of anodic oxidation.
- 10. A thin-film device comprising at least a substrate, a plurality of bus lines provided on said substrate, and connection portions electrically connected to said bus lines, said bus lines and said connection portions being formed of an anodically oxidizable metal and having upper surfaces parallel to said substrate and inclined side surfaces, respectively, said bus lines and said connection portions including inner conducting portions and outer insulating oxide portions formed by anodic oxidation to cover said inner conducting portions, respectively.
- 11. A thin-film device according to claim 10, wherein said thin-film device is a substrate including thin-film transfistors.
- 12. A thin-film device according to claim 11, wherein the substrate including said thin-film transistors is a substrate of a liquid crystal display device, said bus lines are gate bus lines, and said

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connection portions are gate electrodes of said thin-film transistors, said thin-film device further comprising an insulating layer covering said bus lines and said connection portions, a plurality of drain bus lines arranged on said insulating layer to cross said gate bus lines, and a plurality of pixel electrodes.

- 13. A thin-film device according to claim 12, further comprising storage capacitor electrodes arranged on said substrate and made of the same material as said gate bus lines and said connection portions.
- 14. A thin-film device according to claim 10, wherein said thin-film device is an MIM diode.
- 15. A thin-film device according to claim 10, wherein said anodically oxidizable metal comprises at least one selected from the group consisting of Al, Ta, Al-Si, Al-Ta, Al-Zr, Al-Nd, Al-Pd, Al-W, Al-Ti, Al-Ti-B, Al-Sc, Al-Y, Al-Pt, and Al-Pa.
- 16. A thin-film device according to claim 10, wherein the side surfaces of said bus lines and the side surfaces of said connection portions are inclined at angles within the range from 20 degrees to 60 degrees, on average, with respect to said substrate.
- 17. A thin-film device according to claim 16, wherein the side surfaces of said bus lines and the side surfaces of said connection portions are inclined at angles within the range of from 30 degrees to 50 degrees, on average, with respect to said substrate.
- 18. A thin-film device according to claim 10, wherein the side surfaces of said bus lines and the side surfaces of said connection portions are outwardly convex.
- 19 A thin-film device according to claim 10, wherein the angles between the upper surfaces and the side surfaces of said bus lines and of said connection portions are obtuse angles.
- 20. A thin-film device according to claim 10, wherein at least two outer oxide films of said bus lines

and said connection portions contact each other and the contacting outer oxide films electrically isolate the inner conducting portions covered by said contacting outer oxide films.

- wherein a conducting portion separate from said bus lines and said connecting portions is arranged close to said bus lines or said connecting portions; said separate conducting portion includes an inner conducting portion and an outer insulating oxide portion covering said inner conducting portion; the outer oxide film of said separate conducting portion contacts at least one outer oxide film of said bus lines and of said connection portions; and said contacting outer oxide films electrically isolate the inner conducting portions that are covered by said contacting outer oxide films.
- 22. A process for fabricating a thin-film device, said process comprising the steps of:

forming a conducting layer composed of an anodically oxidizable metal on a substrate;

etching said conducting layer in a

predetermined shape;

forming a second oxide film on said conducting layer by anodic oxidation after a first oxide film with a thickness is formed on said conducting layer; and

washing said substrate, whereby said first oxide film is removed by said washing and said second oxide film is not removed by said washing but remains on said conducting layer so as to cover said conducting layer.

- 23. A process according to claim 22, wherein said anodically oxidizable metal includes at least one of Al, Ta, Al-Si, Al-Ta, Al-Zr, Al-Nd, Al-Pd, Al-W, Al-Ti, Al-Ti-B, Al-Sc, Al-Y, Al-Pt, and Al-Pa.
- $n^{-3}$ 24. A process according to claim 22, wherein said first oxide film is one of a naturally oxidized film or a

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hydrated film formed on the surface of said anodically oxidizable metal.

25. A process according to claim 22, wherein said first oxide film has a thickness from 50 nm to 100 nm.

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A process according to claim 22, wherein said washing step is executed using ultrasonic waves of not lower than 200 KHz.

A process according to claim 22, wherein said thin-film device is a substrate including thin-film transistors.

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A process according to chaim 27, further 28. comprising a step for forming an Ansulating film on said substrate and a step for forming a semiconductor layer on said substrate after the second oxide film has been formed, wherein the step for etching said conducting layer forms gate electrodes and gate wirings.

A process according to claim 27, further comprising a step for forming a semiconductor layer on said substrate and a step for forming an insulating film on said substrate prior  $\mathsf{t} \not \! \mathsf{p}$  forming said conducting layer, wherein the step for etching said conducting layer forms gate electrodes and gate wirings.

A process according to claim 22, wherein the step for etching said conducting layer forms gate electrodes having upper surfaces parallel to said substrate and inclined side surfaces.

A process for fabricating a thin-film device, said process comprising the steps of:

forming a semiconductor layer having a predetermined shape on a substrate;

 $f\phi$ rming an insulating film on said substrate to cover said semiconductor layer;

forming a conducting layer composed of an anodically oxidizable metal on said substrate in such a shape as to cover a portion of said semiconductor layer and to form gate electrodes having upper surfaces parallel to said substrate and inclined side surfaces;

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anodically oxidizing said gate electrodes; forming said insplating film into a predetermined shape using said gate electrodes including the anodically oxidized film/as a mask; and injecting impurities into said semiconductor layer using said gate electrodes including said anodically oxidized film and said insulating film as a mask to form an offset in said semiconductor layer. A process according to claim 31, wherein said thin-film device is a substrate including thin-film 10 transistors. A process according to claim 31, wherein said gents given any seem of many least many in the other off off the anodically oxidizable metal includes at least one of Al, Ta, Al-Si, Al-Ta, Al-Zr, Al-Nd, Al-Pd, Al-W, Al-Ti, Al-Ti-B, Al-Sc, Al-Y, Al-Pt, and Al-Pa. 15 34. A process according to claim 31, wherein said anodically oxidized film is a barrier-type anodically oxidized film. A process According to claim 31, wherein said 35. semiconductor layer/comprises a polycrystalline silicone. A process according to claim 31, wherein an [] initial current density at the time of executing the 1:4 anodic oxidation is not smaller than 2.0 mA/cm2 but is not larger than 3.0 mA/cm<sup>2</sup>. 37. A process according to claim 31, wherein the step for forming said gate electrodes comprises the step for forming a gate/electrode layer and the step of patterning the gate electrode layer based on either ionic milling or dry-etching. A process according to claim 31, wherein a 30 masking resist is formed on said conducting layer and is post-baked at a temperature of not lower than 130°C but not higher than 200°C, prior to forming said gate electrode. 39. A thin-film/device comprising a substrate, a 35 semiconductor layer formed in a predetermined shape on

said substrate, an insulating film dovering a portion of said semiconductor layer, a gate electrode formed on said insulating film, and an anodically oxidized film of said gate electrode formed on said insulating film so as to cover said gate electrodes, said anodically oxidized film having a shape as viewed from above which is identical to the shape of said insulating film as viewed from above and having an annular portion in annular contact with said insulating film about said gate electrode, a portion of said semiconductor layer located on the outer side of said insulating film torming a source electrode and a drain electrode, and a portion of said semiconductor layer covered by said annular portion of said anodically oxidized film forming an offset on the inner side of said insulating film.

40. A liquid crystal display device, comprising:

a first substrate comprising the thin-film
device having a plurality of thin-film transistors
according to claim 10 or 39;

substrate; and

d liquid crystal layer filled between the first and second substrates.

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